# A 20 GHz High Speed Mixed Mode Signal R-2R DAC

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**Abstract—** 4-bit high speed R-2R Ladder Digital to Analog Converter (DAC) design is presented in this paper. The high speed DAC design uses a high speed InGaAs/GaAs HEMT device in its summer block. This paper justifies the use of HEMT devices for high speed converter applications. A detailed analysis of the DAC parameters and errors is presented. DAC performance up to 20GHz is presented and it shows very good DNL and INL performance, and stable offset and resolution over the frequency range up to 20 GHz.

**Index terms** - DAC, DNL HEMT, INL, Linearity, Resolution, R-2R ladder, $V_{LSB.}$

## I. INTRODUCTION

THE rapid developments in Radio Frequency (RF) technologies like satellite communication, broadband communication and monolithic microwave integrated circuit (MMIC) have encouraged researchers to develop new high frequency devices described by low noise figures and higher cut-off frequencies. Our research work presented in [1] introduces one such high electron mobility transistor (HEMT) device characterized by its low noise and high frequency operations. The advantages of HEMTS in RF circuits is highlighted by researchers [2], [3], [4], [5]".The dominance of high frequency digital circuits in the RF arena is well established [6]. In order to process digital data for high speed RF digital circuits the analog signals need to be digitally represented and vice versa hence Analog to Digital Convertors (ADC) / DAC's provide an interface to achieve this. The accuracy of digital representation and performance at such high frequencies are critical to the overall system. Hence this paper represents a high frequency DAC using the hetro-junction HEMT presented in [1].

Researchers have used HEMTS to create high frequency RF applications like oscillators [7], [8], [9], [10], programmable decimators [11], optical applications [12], ADC's [13], [14], [15] and high frequency switching applications [16] has been closely studied during the course of the research presented here.There are limited or rare use of HEMTs to realize DACs which was another motivating factor for the authors[17], [18].

This paper is arranged as follows. Section II describes the Digital to Analog Converters and different performance parameters that determine the DAC performance. In Section III, the R-2R ladder DAC implementation is presented and a detailed calculation of the DAC parameters done. Section IV discusses the simulation results which are concluded in Section V.

## II. DIGITAL TO ANALOG CONVERTERS

Digital to Analog Converters (DACs) are an important element of any mixed signal circuit [19]. They are necessary to interface the digital world of the processors with the physical world which recognizes and appreciates signals in the analog domain (sound, light, etc). A DAC converts a digital signal into an equivalent analog signal.

In this paper R-2R DAC is considered. The architecture is as given in Fig. 1 and the Equation 1 defines the output voltage of the DAC for different bit patterns.

$$V_{out} = I.R_f = V_{ref}\left(B_3 + \frac{B_2}{2} + \frac{B_1}{4} + \frac{B_0}{8}\right) \quad \ldots(1)$$

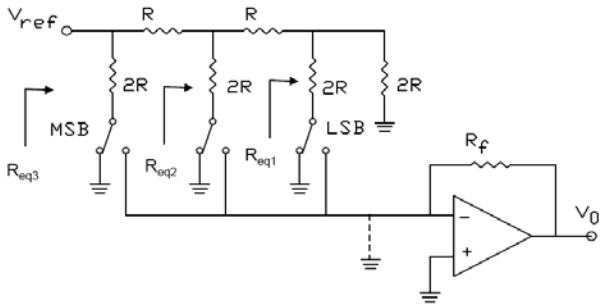


*Figure 1: R-2R Ladder DAC*

The performance of a DAC is evaluated by certain parameters as described in the following:

1. Resolution: It is defined as the amount of variation in the output voltage for every change of the LSB in the digital input. It is a measure of how clearly can we approximate the desired output signal. For an N-bit DAC with reference voltage as $V_{ref}$, resolution is computed by Equation 2 and in Fig. 2

$$Resolution = V_{LSB} = \frac{V_{ref}}{2^N} \quad \ldots(2)$$

2. Reference Voltage: It is defined as a specified voltage used to determine how each digital input will be assigned to each voltage division.
3. Settling Time: It is the time required for the input signal to settle within ±$V_{LSB}$ of the expected output voltage. The concept of settling time is shown in Fig. 3.

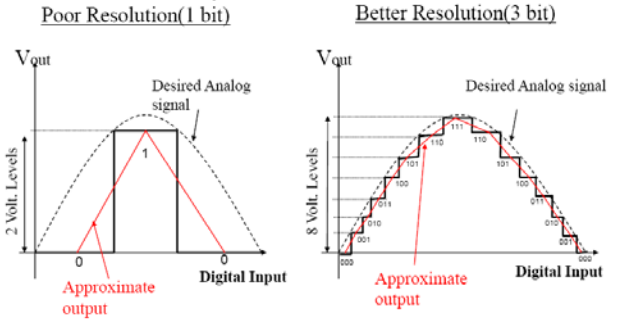


*Figure 2: Resolution of a DAC*

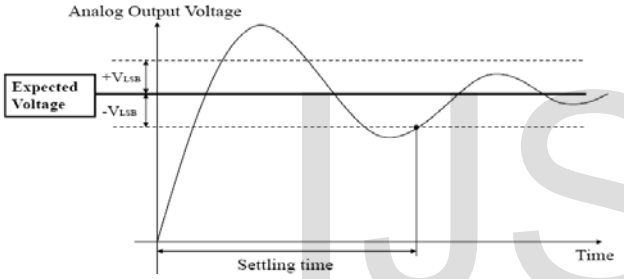


*Figure 3: Settling Time of a DAC*

4. Linearity: It is the difference between the desired analog output and the actual output over the full range of expected values as shown in Fig. 4.

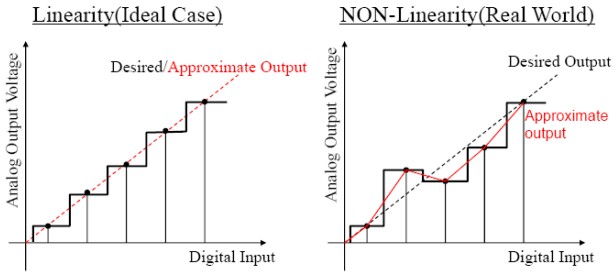


*Figure 4: Linearity of a DAC*

5. Speed: It is the rate of conversion of a single digital input to its analog equivalent and depends on the clock speed of the input signal as well as the settling time of the converter.

The performance evaluation of DAC [20] is also done by the different types of errors as described next:

1. Differential Non-Linearity (DNL): DNL is the difference between an actual step height and the ideal value of 1LSB. Hence if the step height of a DAC is equal to 1LSB, then DNL is zero. If DNL is more than 1 LSB, then the converter can become no-monotonic as in Fig. 5.
2. Integral Non-Linearity (INL): INL is the deviation of the values on the actual transfer function from a best fit straight line as in Fig. 6.
3. Gain Error: It is the difference between the slope of the ideal curve and the actual DAC output as shown in Fig. 7
4. Offset Error: It is the constant voltage difference between the ideal DAC output and the actual output as in Fig. 8.

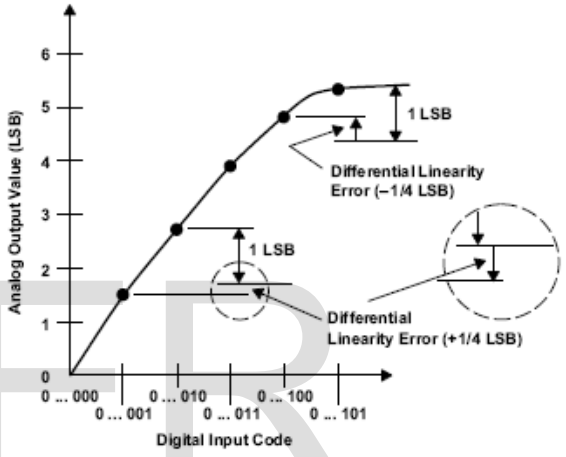


*Figure 5: Differential Non-Linearity of a DAC*

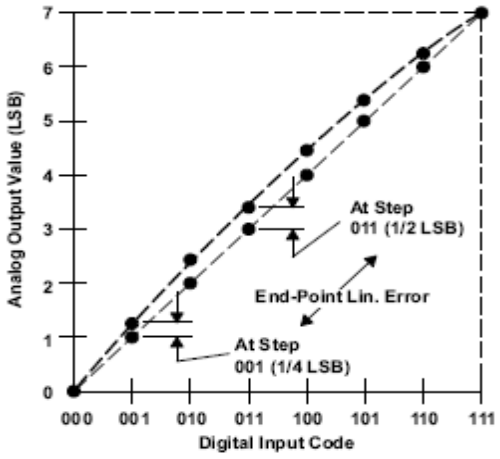


*Figure 6: Integral Non-Linearity of a DAC*

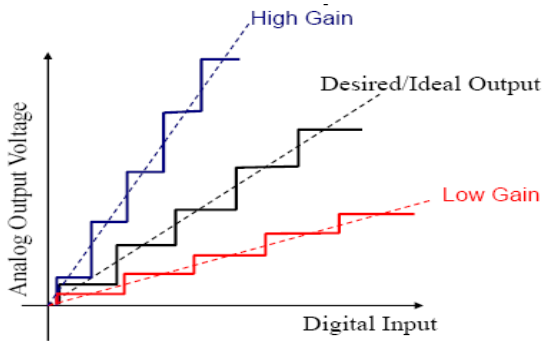


*Figure 7: Gain Error in DAC*

5. Non-Monotonicity: It is the decrease in the output voltage with an increase in the digital input as in Fig. 9.

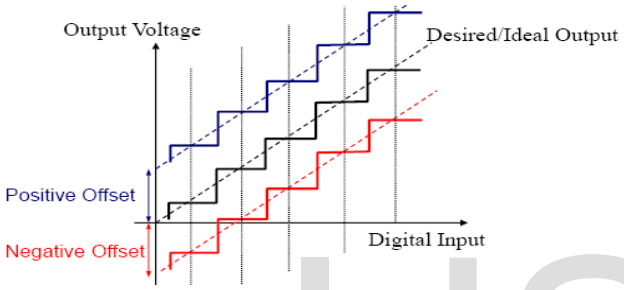


*Figure 8: Offset Error in DAC*

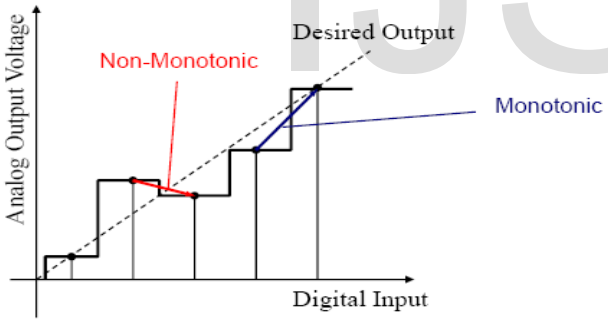


*Figure 9: Non-monotonicity in DAC response*

## III. R-2R Ladder DAC Implementation

### A. Circuit Simulation in Spice:

An R-2R ladder DAC is simulated in Spice Simulator with InGaAs/GaAs HEMT transistor based summer. The design and results of the high speed HEMT transistor were reported in [1]. The circuit schematic for a 4-bit DAC is shown in Figure 10.

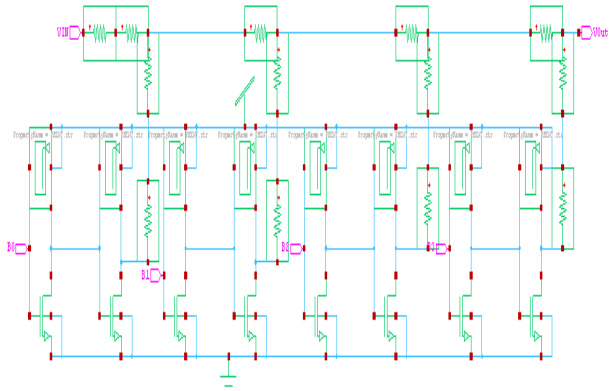

*Figure 10: Circuit Schematic of 4-bit R-2R DAC*

The circuit is simulated using a Spice simulator for all the ranges of 4-bit input patterns ($0000_2$-$1111_2$). The simulation inputs as given in Fig. 11 and 13 are provided in the form of 4 pulse trains representing $b_3$-$b_0$ (MSB-LSB). The frequency of the pulse representing $b_0$ determines the operating frequency of the DAC. The circuit simulation results are presented for a frequency range from 20GHz to 40GHz as shown in Fig. 12 and 14. A linear fit of the output voltage is done for calculating various parameters as described in the next section III B .

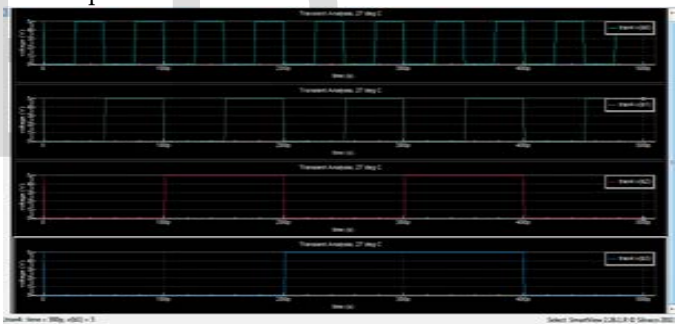

Figure 11: Simulation inputs for 20GHz

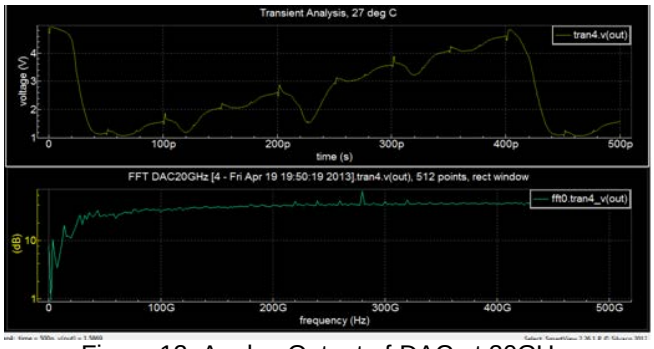


Figure 12: Analog Output of DAC at 20GHz

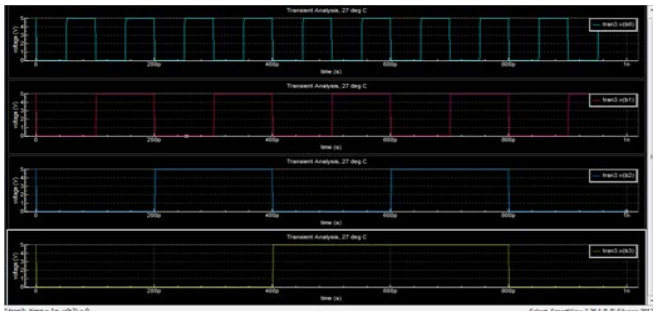

Figure 13: Simulation inputs for 40GHz

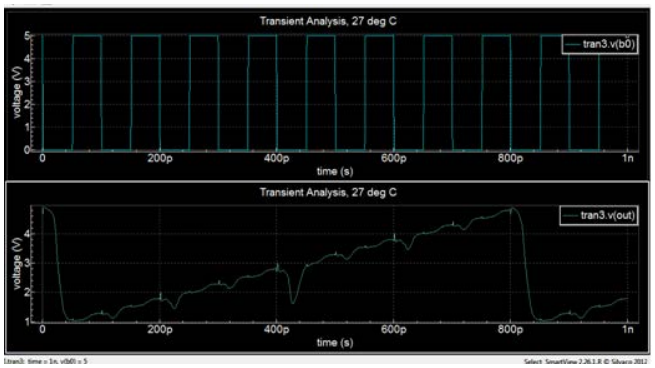


Figure 14: Analog Output of DAC at 40GHz (curve in red is the straight line fit)

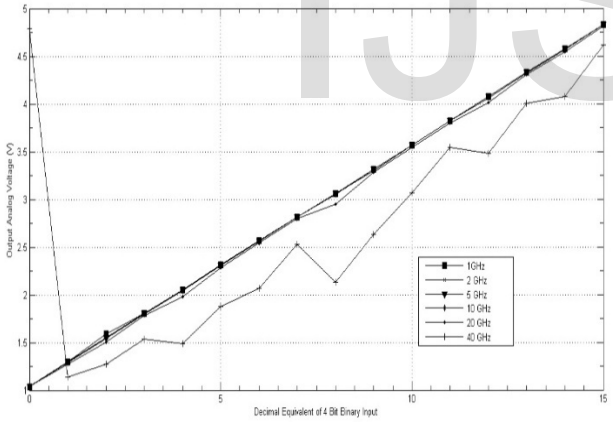


Figure 15: DAC Analog Output for all frequencies

### *B.* DAC Parameter Calculations:

1. Offset, $V_{off}$: Offset Voltage for the design is 1.039V except at 40GHz.

2. Resolution: $V_{ref}$ for the implemented R-2R ladder DAC is 5V. Hence the ideal resolution is given by Equation 4. However, from simulation results it is seen that the DAC offset is 1.039V. Hence the actual resolution of the DAC is given by equation 5 and it can be seen that the resolution is different for different frequencies as tabulated in Table 1.

$$\text{Resolution} = V_{LSB} = \frac{5V}{2^4} = 0.3125V \quad \ldots(4)$$

$$\text{Resolution} = V_{LSB} = \frac{V_{out,max} - V_{out,min}}{2^N} \quad \ldots(5)$$

$$V_{LSB}\,at\ 1GHz = \frac{4.83 - 1.039}{2^4} = 0.237V \quad \ldots(6)$$

3. Linearity: Based on the results shown in Figure 30, the nonlinearity of the DAC at different frequencies is calculated as in Equation 7 and the results are tabulated in Table 1.

$$Linearity = \frac{\Delta V}{Output\ Range} \quad \ldots(7)$$

4. Differential Non-Linearity: DNL is analytically calculated using Equation 8. Calculations are shown for 1GHz frequency and the results for other frequencies are compiled in Table 1.

$$DNL = \max\{V_{out}(i+1) - V_{out}(i) - V_{LSB}\} \quad \ldots(8)$$

$$= 1.594\text{-}1.295\text{-}0.237 = 0.26\ V_{LSB}$$

5. Integral Non-Linearity: INL is computed by using Equation 9. Here, $V_{out}(code)$ is the output voltage at a given binary code and $V_{fit}(code)$ is the output at the same code for a linear fit curve. The calculations for 1GHz are shown in Equation 9. Other results are compiled in Table 1.

$$INL = \max\{V_{out}(code) - V_{fit}(code)\}/V_{LSB} \quad \ldots(9)$$

$$= (1.594\text{-}1.56)/0.237$$

$= 0.14\ V_{LSB}$

6. Monotonicity: Figure 15 shows that the DAC response is monotonically increasing for all frequencies 1 GHz to 20 GHz except at 40GHz. At 40GHz, the DAC, DNL is negative at input values of $0100_2$, $1000_2$ and $1100_2$. Hence, the DAC cannot be used at 40GHz operating frequency.

## IV. Results And Discussion

This section summarizes the results computed in Section III.B.

Table 1
DAC parameters at different operating frequencies

| Freq (GHz) | $V_{off}$ (V) | $V_{LSB}$ (V) | Linearity (%) | DNL (LSB) | INL (LSB) |
|---|---|---|---|---|---|
| 20 | 1.039 | 0.236 | 2.11 | 0.402 | 0.337 |

1. The offset voltage of DAC is a high value of 1.039. However, it is fixed over the entire frequency range under consideration which is a good performance criterion.
2. Resolution of the DAC over the frequency range is constant value and hence, the DAC is usable over the frequency range up to 20GHz.
3. Differential non-linearity and integral non-linearity of the designed DAC are also small fraction of LSB. This shows that the DAC performance over the entire input range is good.
4. As the DAC response for 40GHz is non-monotonic as in Fig. 15, the DAC cannot be used at 40GHz frequency and hence the calculations are not presented at 40GHz and the DAC is usable upto a frequency of 20GHz.

## V. Conclusion

A high speed R-2R ladder 4-bit DAC design using an InGaAs/GaAs HEMT and performance analysis for the same was presented. The HEMT device used was designed for high speed converter applications and was reported in earlier publications. A thorough analysis of the DAC parameters and the calculations of the errors at different operating frequencies are presented in this paper.

The DAC implemented has a unity gain summer designed using the high speed HEMT device, which is used for summing the weighted voltages due to the digital input. The simulation results are presented for 20GHz and 40GHz frequencies.. The analog output follows the input fit a very good linear fit for frequencies up to 20GHz. The DAC response is monotonous up to 20GHz frequencies. The designed DAC is reported to have a worst INL DNL of 0.337LSB and 0.402LSB.

It is concluded that the design based on earlier reported HEMT device is suitable for DAC applications up to 20GHz; the DAC has demonstrated very good linearity and error performance.

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